Remarks

The Official Action rejected claims 1-13 and 27-31. Applicant has amended claims 1-4, 10-12 and 27 and canceled claims 5-9 and 28-31. Claims 39-48 have been newly added. Reconsideration and allowance of the pending claims are respectfully requested.

Claim Rejections under 35 USC 102

The Official Action rejected claims 1, 2 and 11 under 35 USC 102(e) as being anticipated by Dell et al. (US Patent 6,349,390). Applicant respectfully requests reconsideration and withdrawal of the present rejection.

As is well-established, in order to successfully assert a prima facie case of anticipation, the Office Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Office Action has not succeeded in making a prima facie case.

Each of claims 1, 2 and 11 recites a memory device comprising: an interface buffer .... ; and memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array in response to a read command from the memory controller ..... , is unanticipated by Dell.

Dell teaches a memory module attached to a computer system to check and correct memory errors within the module. Figs. 1 and related text teach that the memory module 10 comprises a plurality of memory cells 12a-12i, a bus controller 34, an ECC unit 62, a DSP 36, switches 50 & 52 and other components. Memory buses 14 and 16 couple the memory module 10 to the memory controller 28.

According to Fig. 3 and related text, bus controller 34 monitors the activities on the memory controller 28 and when the memory controller 28 does not request read or write or other operation to or from the memory module 10, bus controller 34 causes the switches 50 and 52 open to disconnect the memory buses and the memory cells, so that DSP of the memory module 10 takes control of the operation of the memory module 10. Then, ECC unit 62 checks memory errors within the memory cells in response to a read command from the DSP (col. 4, lines 33-38). Further, the Office Action regards the memory module 10 as the memory device of claim 1.

In lieu of the above, claim 1 of the present application is unanticipated by Dell, because claim 1 recites the memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array in response to a read command from the memory controller, but not from the DSP within the memory device 10.

Since Dell does not teach each and every limitation of claims 1, 2 and 11, Dell does not anticipate the invention of claims 1, 2 and 11. Applicant respectfully requests the rejection of claims 1, 2 and 11 be withdrawn.

Particularly, Applicant would like to point out that claim 11, which recites the memory device further comprises bus error logic associated with the interface buffer to carry out a check for bus errors in transactions across the first memory bus between the memory controller and the first interface, is unanticipated by Walker.

The Office Action appears to rely on col. 3, lines 23-64 of Walker for the teaching of the bus error logic. Applicant respectfully submits that the prima facie case of anticipation requires the Office Action to provide a single prior art document that includes every element and limitation of the claim or claims being rejected.

However, the Office Action rejects claim 1 in view of prior art Dell, but rejects claim 11 including claim 1 as a base claim in view of prior art Walker, which does not meet the requirement of prima facie case of anticipation.

Further, col. 3, lines 23-64 of Walker teaches the host controller 13 comprises error detection and correction logic to check and correct memory errors in DIMMs, but not bus errors in transactions across the memory bus. Walker is silent on a bus error logic within the memory device that checks bus errors in transactions across the memory bus between the memory controller and the memory device.

Moreover, since Applicant has changed the subject matter of claim 1 from "memory system" back to "memory device", Applicant would like to point out the unanticipatability of the amended claim 1 over Walker, in order to expedite the prosecution.

The Office Action mailed on September 6, 2006 alleged that the memory device of Walker comprises all of the components of Fig. 6. With this allegation, Walker teaches the memory error logic (ECC units 62a-62e) carries out the check of memory errors within the memory subsystem 40 in response to a read command from the read/write control logic 66 within the memory device, but not from the memory controller that is external to the memory device, as required by claim 1. In particular, the read/write control logic 66 makes the read command to read check bits from the memory subsystem 40 for memory error checking and correction based upon a cleansing instruction initiated by the cleansing logic 70 within the memory device.

The Final Office Action mailed on March 01, 2007 (opinion 20 on page 7) appears to rely on col. 3, lines 36-57 of Walker for the teaching of the memory controller and rely on col. 4, lines 27-45 and col. 8, lines 46-51 of Walker for the

teaching of the memory device. In lieu of this, the Final Office Action appears to regard the host controller13 as the memory controller and regard memory subsystem 40 as the memory device. With this assumption, Walker teaches the memory error logic (ECC units 62a-62e) is included by the memory controller. However, claim 1 recites that a memory device comprising an interface buffer .... ; and memory error logic associated with the interface buffer. In other words, claim 1 requires that the memory error logic is included by the memory device, but not by the memory controller.

Claim Rejections under 35 USC 103 (Walker/Goris)

The Official Action rejected claims 3-10, and 12 under 35 USC 103(a) as being unpatentable over Dell in further view of Goris (US Patent Application 2002/0167791).

Claims 5-9 have been canceled. Claims 3-4 and 12 include claim 1 as a base claim. Therefore, claims 3-4 and 12 are allowable for the similar reason proffered for claim 1. Applicant respectfully requests reconsideration and withdrawal of the present rejection.

Claims 27-30

The Official Action rejected claims 3-10, and 12 under 35 USC 103(a) as being unpatentable over Dell in further view of Goris (US Patent Application 2002/0167791).

Claims 28-30 have been canceled. Claim 27 is neither taught nor suggested by the combination of Walker and Goris for the following reasons:

As discussed in M.P.E.P 2143.03, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior

art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

For similar reasons proffered for claim 1, Walker does not teach a first memory device having a first interface buffer, wherein the first interface buffer provides a first memory error logic to carry out a check for memory errors within the first storage array in response to a first read command from the memory controller. Goris teaches a system having a receiver connecting to a number of storage cards. However, Goris is silent on memory error logic to check memory errors within the first storage array.

Since the combination of Walker and Goris does not teach each and every limitation of claim 27, claim 27 is patentable over Walker in further view of Goris. Therefore, claim 27 is allowable and withdrawal of the present rejection is respectfully requested.

Newly Added Claims

The Applicants have added claims 39-48. Each of claims 39-45 includes one of the allowable claims 1 and 27 as a base claim and therefore is allowable too.

Each of claims 46-48 contains limitations not disclosed, taught, or suggested by the cited art. In particular, each of claims 43-45 recites a method comprising: receiving a read command from a memory controller; retrieving a check bit from a storage array of the memory device, in response to the read command; and utilizing the check bit to check memory errors within the storage array, by a memory error logic of the memory device.

For similar reasons proffered for claim 1, the cited references fail to disclose, teach, or suggest the method requested by claims 46-48.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that all remaining claims are in condition for allowance. Reconsideration is requested, and allowance of all remaining claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

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